ARSD College, University of Delhi

Model Course Handout/Lesson Plan

Course Name: Computer System Architecture					**B.Sc. (Hons.) Computer Science**	
Semester	**Course Code**	**Course Title**	**Lecture (L)**	**Tutorial (T)**	**Practical (P)**	**Credit (C)**
I	32341102	Core Course-DSC-2 (BHCS02)- Computer System Architecture	4 credit-4	0	4 credit-2	6
Teacher/Instructor(s)		Uma Ojha				
Session		2021-22				

Course Objective:

This course introduces the students to the fundamental concepts of digital computer organization, design and architecture. It aims to develop a basic understanding of the building blocks of the computer system and highlights how these blocks are organized together to architect a digital computer system.

Course Learning Outcomes:

On successful completion of the course, students will be able to:

1. Design Combinational Circuits using basic building blocks. Simplify these circuits using Boolean algebra and Karnaugh maps. Differentiate between combinational circuits and sequential circuits.
2. Represent data in binary form, convert numeric data between different number systems and perform arithmetic operations in binary.
3. Determine various stages of instruction cycle and describe interrupts and their handling.
4. Explain how CPU communicates with memory and I/O devices.
5. Simulate the design of a basic computer using a software tool

Lesson Plan

Unit No.	Learning Objective	Week No.	Topics to be covered
I	Digital Logic Circuits	1	Introduction: Digital Logic Gates, Flipflops and their characterstic table, Logic circuit simplification using Boolean Algebra and
		2	Karnaugh Map, Don't Care conditions. Combinational Circuits, Sequential Circuits.
II	Digital Components	3	Decoders, Encoders, Multiplexers, Binary Adder
		4	Binary Adder- Subtractor, Binary Incrementer, Registers and Memory Units
III	Data Representation	5	Binary representation of data, representation of alpha data, representation of numeric data in different number systems, conversion between number systems, complements, representation of decimal numbers,
		6	Representation of signed and unsigned numbers, addition and subtraction of signed and unsigned numbers and overflow detection.
IV	Operations and Control	7	Arithmetic and logical micro-operations, micro programmed control vs. hardwired control, instruction format, instruction set completeness, timing and control, instruction cycle
		8-9	Memory reference instructions and their implementation using arithmetic, logical, program control, transfer and input output micro operations
		10	Interrupt Cycle
V	Instructions	11-12	Instruction format illustration using single accumulator organization, general register organization and stack organization, Addressing Modes, zero-address instructions, one-address instructions, two- address instructions and

			three-address instructions,
VI	Pipeline and Vector Processing	13	Parallel Processing and Pipelining
VII	Peripheral Devices	14	I/O interface, I/O vs. Memory Bus, Isolated I/O, Memory Mapped I/O
		15	Direct Memory Access

Evaluation Scheme:

No.	Component	Duration	Marks
1.	Internal Assessment		25
	• Quiz		
	• Class Test		
	• Attendance		
	• Assignment		
2.	End Semester Examination	3 hrs.	75

Details of the Course		
Unit	**Contents**	**Contact Hours**
I	Digital Logic Circuits: Logic Gates, truth tables, Boolean Algebra, digital circuits, combinational circuits, sequential circuits, circuit simplification using Karnaugh map, Don't Care Conditions, flip-flops, characteristic tables	10
II	Digital Components: Half Adder, Full Adder, Decoders, Multiplexers, Registers and Memory Units	6
III	Data Representation and Basic Computer Arithmetic: Number system, complements, fixed and floating point representation. Alphanumeric representation. Addition, subtraction.	9
IV	Basic Computer Organization and Design: Common Bus system, instruction codes, instruction format, instruction set completeness, Sequence Counter, timing and control, instruction cycle, memory	14

	reference instructions and their implementation using arithmetic, logical, program control, transfer and input output micro-operations, interrupt cycle.	
V	Central Processing Unit: Micro programmed Control vs Hardwired Control, lower level programming languages, Instruction format, accumulator, general register organization, stack organization, zero-address instructions, one-address instructions, two-address instructions, three- address instructions, Addressing Modes, RISC, CISC architectures, pipelining and parallel processing.	10
VI	Pipeline and Vector Processing	3
VII	Memory Organization and Input-Output Organization: Input-Output Organization: Peripheral Devices, I/O interface, I/O vs. Memory Bus, Programmed I/O, Interrupt-Driven I/O, Direct Memory Access	8
	Total	**60**

S. No.	**Name of Authors/Books/Publishers**	**Year of Publication /Reprint**
1.	Mano, M. Computer System Architecture. 3rd edition. Pearson Education.	1992
2.	Mano, M. Digital Design. Pearson Education Asia.	1995
3.	Stallings, W. Computer Organization and Architecture Designing for Performance 8th edition. Prentice Hall of India.	2010
4.	Null, L., & Lobur, J. The Essentials of Computer Organization and Architecture. 5th edition. (Reprint) Jones and Bartlett Learning.	2018
Mode of Evaluation: Internal Assessment / End Semester Exam		