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Roll No. | | | | | | | | | | | |

S. No. of Question Paper : 2295

Unique Paper Code : 42344403 IC

Name of the Paper : Computer System Architecture

Name of the Course : B.Sc. (Programme) (Physical Sciences/Mathematical Sciences)

Semester : IV

Duration : 3 Hours Maximum Marks : 75

(Write your Roll No. on the top immediately on receipt of this question paper.)

Question No. 1 is compulsory.

Attempt any *five* questions from Section B.

Section A

(Compulsory)

1. (*a*) Obtain 10's complement of the six-digit decimal number 909951. 1

P.T.O.

(*b*) Given the following : 2

$$R3 \leftarrow R1 + (R2)' + 1$$

Specify the output of this micro-operation.

(*c*) List the instructions needed in the basic computer in order to set E flip-flop to 1. 2

(*d*) Differentiate between a positive and a negative edge triggered flip-flop. 2

(*e*) What is a Binary counter ? How many flip-flops will be required for an n-bit binary counter ? 2

(*f*) Convert the following numbers with the indicated bases to decimal : 2

(*i*) $(12121)_3$

(*ii*) $(4310)_5$.

(*g*) Give the characteristic table of JK flip-flop. 2

(*h*) Simplify the following expression using Boolean algebra (Show all the steps) : 2

$$(B.C' + A'.D) . (A.B' + C.D')$$

(e) Differentiate between RAM and ROM. 2

(g) Using zero address instructions, write a program to evaluate the following arithmetic statement : 3

$$X = (A + B) * (C + D)$$

(h) What do you understand by DMA ? Explain the process of DMA transfer. 3

(i) Explain why the following micro-operation cannot be executed during a single clock pulse : 3

DR ← DR + AC (AC does not change)

Specify the sequence of micro-operations performed to execute it.

Section B

(Attempt any *five* questions)

2. (a) Simplify the Boolean function F together with don't care conditions *d* in the sum of products form : 6

$F(w, x, y, z) = \Sigma (0, 1, 2, 3, 7, 8, 10)$

$d(w, x, y, z) = \Sigma (5, 6, 11, 15)$

Implement F using minimal number of NAND gates.

(b) The content of AC in the basic computer is hexadecimal A675 and the initial value of E is 1. Determine the contents of AC, E, PC, AR and IR in hexadecimal after the execution of the CMA instruction (7200). The initial value of PC is hexadecimal 072. 4

3. (a) Draw a block diagram to construct a 5-to-32 line decoder with four 3-to-8 line decoders and one 2-to-4 line decoder. 5

(b) An instruction is stored at location 300 with address field at location 301. The address field has the value 400. A process register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is : 5

(i) Direct

(ii) Immediate

(iii) Relative

(iv) Register Indirect

(v) Index with R1 as the index register.

4. (a) What is a half adder ? Give its function table. Design a 4-bit binary incrementer using half-adders. 6

(b) Convert as directed : 4

(i) $(11000011.10101)_2 = (?)_{16}$

(ii) $(736)_8 = (?)_{10}$

5. (a) The contents of Register A and Register B are 11001100 and 00110011 respectively. List the contents of Register A if the following operations are carried out on contents of A using contents of B : 6

(i) Selective Complement

(ii) Masking

(iii) Selective Set.

(b) Write the micro-operations performed to execute the following instructions : 4

(i) BSA

(ii) AND to AC.

6. (a) Explain the three different types of instruction formats. Given the following instructions (in hexadecimal), identify the category to which they belong : 5

(i) 7800

(ii) F800.

(b) Perform the following arithmetic operation using signed 2's complement representation for negative numbers : 3

$$(-38)_{10} - (+85)_{10}$$

(c) How many address lines and input-output data lines are needed for a memory unit of 16M words × 32 bits per word ? 2

7. (a) What is a multiplexer ? Explain the working of 4-to-1 MUX with a suitable diagram. 5

(b) Find the hexadecimal equivalent of $(189.75)_{10}$. 2

(c) List the micro-operations performed during fetch & decode phase of an instruction. 3

8. (*a*) Differentiate between : 4

(*i*) Isolated I/O and memory mapped I/O

(*ii*) Synchronous and Asynchronous Data Transfer

(*b*) Design a combinatorial circuit with three inputs *x*, *y*, *z* and three outputs A, B, C. When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input; otherwise the binary output is one less than the input. 6